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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,350	03/07/2001	Chun Hsiang Lai	JCLA6643	4896
7590 J. C. Patents, Inc. 4 Venture Suite 250 Irvine, CA 92618				
EXAMINER				
NADAV, ORI				
ART UNIT		PAPER NUMBER		
2811				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

09/801,350

**Applicant(s)**

LAI ET AL.

**Examiner**

Ori Nadav

**Art Unit**

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 31 March 2011.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4, 13 and 15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 13 and 15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-896)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woods (3,594,584) or Switsen (3,771,017) or White (4,007,399), all in view of Lin (5,982,601).

Regarding claims 1-2 and 13, Woods teaches in figure 12 and related text a protection circuit comprising:

a silicon controlled rectifier (SCR) circuit (the circuit including SCR 187), which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively and directly connected to an I/O pad and a ground voltage, so as to discharge the electrostatic charges; and

an anti-latch-up circuit (the circuit which includes in part elements 182, 183, 177) which comprises a fourth connection terminal directly connected to a voltage source, a fifth connection terminal directly coupled to the ground voltage, and a sixth connection terminal directly connected to the third connection terminal of the SCR circuit, and

a first diode (173 or 181 or 184) having a first input end coupled to the I/O pad and a second input end coupled to the fourth connection terminal, wherein when the first diode is not conducted, the anti-latch-up circuit substantially generates an anti-latch-up signal to the third connection terminal of the SCR circuit according to the voltage source so as to prevent latching up of the SCR circuit during normal operation, and when the first diode is conducted, the anti-latch-up circuit does not substantially generate the anti-latch-up signal, and

a second diode (any other diode), having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad, and

wherein the anti-latch-up signal sent from the sixth connection terminal to the SCR circuit comprises a voltage signal.

Although Woods does not explicitly state an I/O pad, this feature is inherent in Wood's device because the device requires an I/O pad in order to provide external connection to the device.

Woods does not explicitly state that when the first diode is not conducted, the anti-latch-up circuit substantially generates an anti-latch-up signal to the third connection terminal of the SCR circuit according to the voltage source so as to prevent latching up of the SCR circuit during normal operation, and when the first diode is conducted, the anti-latch-up circuit does not substantially generate the anti-latch-up signal, and does not teach using the device in an electrostatic discharge (ESD) protection circuit.

Regarding claims 1-2 and 13, Switsen teaches in figure 1 and related text a protection circuit comprising:

a silicon controlled rectifier (SCR) circuit (the circuit including SCR), which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively and directly connected to an I/O pad and a ground voltage, so as to discharge the electrostatic charges; and

an anti-latch-up circuit (the circuit which includes in part element 16 or 30, 32) which comprises a fourth connection terminal directly connected to a voltage source, a fifth connection terminal directly coupled to the ground voltage, and a sixth connection terminal directly connected to the third connection terminal of the SCR circuit, and

a first diode (18 or 28) having a first input end coupled to the I/O pad and a second input end coupled to the fourth connection terminal, wherein when the first diode is not conducted, the anti-latch-up circuit substantially generates an anti-latch-up signal to the third connection terminal of the SCR circuit according to the voltage source so as to prevent latching up of the SCR circuit during normal operation, and when the first diode is conducted, the anti-latch-up circuit does not substantially generate the anti-latch-up signal, and

a second diode (any other diode), having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad, and

wherein the anti-latch-up signal sent from the sixth connection terminal to the SCR circuit comprises a voltage signal.

Although Switsen does not explicitly state an I/O pad, this feature is inherent in Switsen's device because the device requires an I/O pad in order to provide external connection to the device.

Switsen does not explicitly state that when the first diode is not conducted, the anti-latch-up circuit substantially generates an anti-latch-up signal to the third connection terminal of the SCR circuit according to the voltage source so as to prevent latching up of the SCR circuit during normal operation, and when the first diode is conducted, the anti-latch-up circuit does not substantially generate the anti-latch-up signal, and does not teach using the device in an electrostatic discharge (ESD) protection circuit.

Regarding claims 1-2 and 13, White teaches in figure 1 and related text a protection circuit comprising:

a silicon controlled rectifier (SCR) circuit (the circuit including SCR 120), which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively and directly connected to an I/O pad and a ground voltage, so as to discharge the electrostatic charges; and

an anti-latch-up circuit (the circuit which includes in part elements 110, 123 or 112, 124) which comprises a fourth connection terminal directly connected to a voltage source, a fifth connection terminal directly coupled to the ground voltage, and a sixth connection terminal directly connected to the third connection terminal of the SCR circuit, and

a first diode (129 or 116) having a first input end coupled to the I/O pad and a second input end coupled to the fourth connection terminal, wherein when the first diode is not conducted, the anti-latch-up circuit substantially generates an anti-latch-up signal to the third connection terminal of the SCR circuit according to the voltage source so as to prevent latching up of the SCR circuit during normal operation, and when the first diode is conducted, the anti-latch-up circuit does not substantially generate the anti-latch-up signal, and

a second diode (any other diode), having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad, and

wherein the anti-latch-up signal sent from the sixth connection terminal to the SCR circuit comprises a voltage signal.

Although White does not explicitly state an I/O pad, this feature is inherent in White's device because the device requires an I/O pad in order to provide external connection to the device.

White does not explicitly state that when the first diode is not conducted, the anti-latch-up circuit substantially generates an anti-latch-up signal to the third connection terminal of the SCR circuit according to the voltage source so as to prevent latching up of the SCR circuit during normal operation, and when the first diode is conducted, the anti-latch-up circuit does not substantially generate the anti-latch-up signal, and does not teach using the device in an electrostatic discharge (ESD) protection circuit.

Lin teaches in figures 6, 9 and 10 and related text connections to voltage  $V_h$  or to an I/O pad, wherein the device is used in an electrostatic discharge (ESD) protection circuit. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use any of prior art's devices as an electrostatic discharge (ESD) protection circuit by providing connections to a voltage or to an I/O pad, such that when the first diode is not conducted, the anti-latch-up circuit substantially generates an anti-latch-up signal to the third connection terminal of the SCR circuit according to the voltage source so as to prevent latching up of the SCR circuit during normal operation, and when the first diode is conducted, the anti-latch-up circuit does not substantially generate the anti-latch-up signal, and does not teach using the device in an electrostatic discharge (ESD) protection circuit, in order to provide proper protection to the circuit, when using the device as an electrostatic discharge (ESD) protection circuit.

Regarding claims 3 and 4, Lin teaches in figure 5 an SCR circuit comprises: a P-type substrate; an N well, formed in the p-type substrate; a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage GND; a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage GND; a second N+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, and coupled via the third connection terminal of SCR circuit to the sixth connection terminal of the anti-latch-up circuit A, serving as a guard ring to collect electrons to avoid latch up when the anti-latch-up circuit sends signal through the sixth connection terminal to the third



connection terminal of the SCR circuit during normal operation, and floating when the anti-latch-up circuit sends no signal to the SCR circuit during an ESD event;  
a second P+ doped region, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/O pad 1; and a third N+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source (the pad line),

wherein Lin teaches in figure 6C an anti-latch-up circuit comprises: a capacitor C, having a first contact end and a second contact end, respectively coupled to the second N+ doped region and the ground voltage, and a resistor R, having a first end and a second end, respectively coupled to the voltage source and the second N+ doped region.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's device as taught by Lin, in order to improve the protection capabilities of the device.

Regarding claim 15, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse in prior art's device in order to improve the protection capabilities of the device.

***Response to Arguments***

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References C-J are cited as being related to SCR protection circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

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information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.  
4/25/2011

/ORI NADAV/  
PRIMARY EXAMINER  
TECHNOLOGY CENTER 2800